REMARKS

Claims 1-11 are pending in the above-identified application. Claims 1, 3, 8, and 9 are independent.

Claim Rejection – 35 USC 112

Claims 1 and 2 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. In particular, claim 1 is considered indefinite because the phrase "a testing device for a semiconductor integrated circuit which incorporates a multiple number of D/A converters" is not clear as to whether the semiconductor integrated circuit or testing device incorporates the D/A converters. Applicant respectively traverses this rejection.

First of all and as can be seen in Figure 3, both the LCD driver (i.e., semiconductor integrated circuit) and the voltage generator (i.e., part of the testing device) have D/A converters (e.g., see claim 2). They both provide analog voltage signals to the differential amplifier array module 4. In any case, in order to clarify that the output voltage output from each of the output terminals is from the LCD driver to be tested (the claimed semiconductor integrated circuit), claim 1 has been amended to recite that the output terminals stated in the claim preamble are associated with the semiconductor integrated circuit. As claim 1 as amended, is definite, Applicant respectfully requests that the rejection be withdrawn.

Claim Rejecti n – 35 USC 103; Yamagami, Paulos, Ohya

Claim 1 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagami et al. (U.S. Patent 6,121,786) in view of Paulos et al. (U.S. Patent 6,091,350) and Ohya (U.S. Patent 5,745,064). Applicant respectfully traverses this rejection.

Claim 1 is directed to a testing device for a semiconductor integrated circuit. The semiconductor integrated circuit outputs voltages via output terminals. A reference voltage generator sequentially generates a multiple number of reference voltages to be compared to each output voltage output from each of the output terminals. Differential amplifiers, each receiving the output voltage output from an associated output terminal and receiving the reference voltage from the reference voltage generator. A comparator receives amplified output voltages from the multiple number of differential amplifiers and judges whether the amplified output voltages from each from each of the differential amplifiers falls within a given voltage range.

The arrangement of the present invention enables the reference voltage generator to be commonly used for testing of different kinds of LCD driver LSIs, each having different tonal output level sets. In other words, the reference voltage generator is able to sequentially generate a desired tonal voltage when multiple pieces of digital data corresponding to the standard multiple tonal voltages to be output from the LCD driver under test are sequentially supplied to the reference voltage generator (present specification, page 9).

Yamagami is directed to a semiconductor integrated circuit which, among other things, contains circuitry for carrying out a "burn-in test." Yamagami's circuit uses two kinds of power supply voltages in order to switch the power supply voltage applied to the tested circuit according to the nature of the test. Thus, during the operation margin certification test, the internal power supply voltage exhibits continuously varying characteristics. During an accelerated test, a voltage can be increased at a sufficiently high rate. The test accommodates testing over a range of voltages for a predetermined period of time at a high temperature.

In particular, Yamagami discloses a semiconductor integrated circuit that includes an internal voltage step-down circuit that can supply different internal power supply voltages suitable for the burn-in test. The internal voltage step-down circuit includes a reference voltage generator 1 for generating a plurality of reference voltages. The reference voltage generator 1 generates two types of reference voltages VREF1 and VREF2 and outputs these voltages to first and second internal power supply circuits 5 and a reference voltage comparator 8. Each of the first and second internal power supply circuits includes a differential amplifier 7. The reference voltage comparator 8 receives both reference voltages VREF1 and VREF2 and compares them with each other.

The Office Action alleges that Yamagami's reference voltage generator 1 teaches the claimed reference voltage generator, differential amplifiers 7 teach the

claimed differential amplifiers, and reference voltage comparator 8 teaches the claimed comparator.

However, the claimed voltage generator sequentially generates n-levels of reference voltages (i.e., one voltage level at a time), whereas Yamagami's voltage generator generates two reference voltages VREF1 and VREF2. Thus, Applicant submits that Yamagami fails to teach or suggest at least the claimed reference voltage generator. Also, the claimed comparator receives amplified output voltages from the differential amplifiers, whereas the comparator of Yamagami compares reference voltages. Thus, Applicant submits that Yamagami fails to teach or suggest at least the claimed comparator. Accordingly, at least for these reasons, Applicant submits that the rejection fails to establish *prima facie* obviousness for claim 1.

The Office Action relies on Ohya for teaching multiple D/A converters which output voltages. However, Ohya also does not teach or suggest at least the claimed reference voltage generator and comparator. Thus, Ohya does not make up for the deficiency in Yamagami.

The Office Action relies on Paulos for teaching selectively outputting a range of voltages based on a given input voltage. However, Paulos also does not teach or suggest at least the claimed reference voltage generator and comparator. Thus, Paulos does not make up for the deficiency in Yamagami.

Applicant respectfully requests that the rejection be withdrawn.

Claim Rejection – 35 USC 103; Yamagami, Paulos, Ohya, and Cheng

Claim 2 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagami et al. (U.S. Patent 6,121,786) in view of Paulos et al. (U.S. Patent 6,091,350) and Ohya (U.S. Patent 5,745,064), and further in view of Cheng.

Cheng is relied on for teaching D/A converters to generate reference voltages. Applicant submits, however, that Cheng also does not teach or suggest the claimed reference voltage generator which sequentially generates a multiple number of reference voltages. Thus, at least for this reason, Applicant submits that Cheng does not make up for the deficiency in Yamagami. Applicant respectfully requests that the rejection be withdrawn.

Claim Rejection – 35 USC 103; Yamagami, Ohya, Yoshizawa

Claims 3, 4, and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagami, Ohya, and further Yoshizawa et al. (U.S. Patent 4,980,639).

Claim 3 is comparable to claim 1 in the sense that it also recites a reference voltage generator which sequentially generates a multiple number of reference voltages to be compared to output voltages from output terminals of the semiconductor integrated circuit. Claim 8 recites a reference voltage generator which sequentially generates a multiple number of reference voltages, and a step of calculating the difference between the reference voltage generated from the reference voltage generator and the output voltage output from each output terminal in a semiconductor integrated circuit. At least for the same reason in the

above for claim 1, Applicant submits that Yamagami fails to teach or suggest at least the claimed reference voltage generator, as well as the associated step of calculating the difference between the reference voltage generated from the reference voltage generator and the output voltage from each output terminal.

Yoshizawa is relied on for teaching calculating the difference between a predetermined voltage generated from the reference voltage generator and the output voltage from the output terminal. Yoshizawa's reference voltage source 38C produces a reference voltage. Applicant submits, however, that Yoshizawa fails to make up for the deficiency in Yamagami of a reference voltage generator which sequentially generates a multiple number of reference voltages. Thus, Applicant submits that the rejection fails to establish *prima facie* obviousness for claims 3, 4, and 8. Accordingly, Applicant respectfully requests that the rejection be withdrawn.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the various rejections and allowance of claims 1-11 is respectfully requested.

Should the Examiner have any questions concerning this application, the Examiner is invited to contact Robert W. Downs (Reg. No. 48,222) at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No.

02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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